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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,064	02/11/2004	Jae-Hyun Kim	SAM-0517	2101

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/776,064	KIM ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-20 and 22-26* is/are rejected.

7)☒ Claim(s) *8 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11 February 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 4, 5, 6, 7, 10, and 13 are rejected under 35 U.S.C. 102(a, b) as being anticipated by Hayashi et al. (USPN 5,717,251).

3. In reference to claim 1, Hayashi et al. (USPN 5,717,251, hereinafter referred to as the "Hayashi" reference) discloses a method of fabrication which meets the claim. Figures 7A-7F illustrate a method of fabricating a semiconductor device. A passivation layer (44) is provided on a circuit element (45b) of the semiconductor device. The passivation layer (44) is patterned to expose an upper surface of the circuit element (45b). A photosensitive layer (46) is provided on the passivation layer (44) and the circuit element (45b). A photoresist layer (47) is provided on the photosensitive layer (46). A region of the photoresist layer (47) and the photosensitive layer (46) is exposed over the circuit element (45b). The photoresist layer (47) and the exposed region of the photosensitive layer (46) are removed.

4. With regard to claim 3, the passivation layer (44) is selectively etched (figure 7A) to expose the circuit element (45b).

5. With regard to claim 4, a dielectric layer (42) is provided on the semiconductor substrate (41). The circuit element (45b) is provided on the dielectric layer (42).

6. In reference to claims 5 and 6, the circuit element (45b) is a wiring metal layer and is therefore a conductive element (column 10, lines 29-36).

7. With regard to claim 7, the photosensitive layer (46) is a polyimide (column 10, lines 41-45).

8. In reference to claim 10, the photoresist layer (47) and the exposed region of the photosensitive layer (46) are removed by using a developer (column 11, lines 12-14).

9. With regard to claim 13, the photoresist layer (47) protects regions of the photosensitive layer (46), other than the region above the circuit element (45b), from exposure during the exposure step.

10. Claims 14, 16, 17, 18, 19, 20, and 23-26 are rejected under 35 U.S.C. 102(a, b) as being anticipated by Hayashi et al. (USPN 5,717,251).

11. In reference to claim 14, Hayashi et al. (USPN 5,717,251, hereinafter referred to as the "Hayashi" reference) discloses a semiconductor device which meets the claim. Figures 7A-7F illustrate a semiconductor device. A passivation layer (44) is provided on a circuit element (45b) of the semiconductor device. The passivation layer (44) is patterned to expose an upper surface of the circuit element (45b). A photosensitive layer (46) is provided on the passivation layer (44) and the circuit element (45b). A photoresist layer (47) is provided on the photosensitive layer (46). A region of the photoresist layer (47) and the photosensitive layer (46) is exposed over the circuit

element (45b). The photoresist layer (47) and the exposed region of the photosensitive layer (46) are removed.

12. With regard to claim 16, the passivation layer (44) is selectively etched (figure 7A) to expose the circuit element (45b).

13. With regard to claim 17, a dielectric layer (42) is provided on the semiconductor substrate (41). The circuit element (45b) is provided on the dielectric layer (42).

14. In reference to claims 18 and 19, the circuit element (45b) is a wiring metal layer and is therefore a conductive element (column 10, lines 29-36).

15. With regard to claim 20, the photosensitive layer (46) is a polyimide (column 10, lines 41-45).

16. In reference to claim 23, the photoresist layer (47) and the exposed region of the photosensitive layer (46) are removed by using a developer (column 11, lines 12-14).

17. With regard to claim 26, the photoresist layer (47) protects regions of the photosensitive layer (46), other than the region above the circuit element (45b), from exposure during the exposure step.

18. In reference to claims 24 and 25, the examiner notes the process limitations regarding the use of developer such as TMAH in conjunction with the removal of the photoresist. However, this places claims 21, 24, and 25 into the form of **product-by-process claims**:

> Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi* et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in " product by process"

> claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claims 24 and 25 do not distinguish over the Hayashi reference regardless of the process used to remove the photoresist layer and photosensitive layer, because only the final product is relevant, and not the process of making such as the removal of the photoresist layer by using TMAH.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (USPN 5,717,251) in view of Wolf ("Silicon Processing for the VLSI Era, Volume 2 – Process Integration," p.273-275).

21. In reference to claim 2, Hayashi does not disclose the use of a passivation layer made of a stacked CVD oxide layer and a stacked CVD nitride layer. However the use of such a composite passivation layer is well known in the art. Wolf ("Silicon Processing for the VLSI Era, Volume 2 – Process Integration," p.273-276, hereinafter referred to as the "Wolf 2" reference) discloses that a passivation layer made of a stacked CVD oxide layer and a stacked CVD nitride layer (p.275) has the benefits of protecting against mechanical stress, handling, humidity, and mobile ions. Wolf 2 further discloses that these are desirable properties for a passivation layer (p.276). In view of Wolf 2, it would

therefore be obvious to use a passivation layer made of a stacked CVD oxide layer and a stacked CVD nitride layer in the device of Hayashi.

22. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (USPN 5,717,251).

23. With regard to claim 9, Hayashi teaches all of the claimed invention except for the exact thickness of the photoresist layer. Although the Hayashi device does not teach the exact thickness as that claimed by Applicant:

> Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).
>
> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Therefore claim 9 is not patentably distinguishable over the Hayashi reference.

24. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (USPN 5,717,251) in view of Wolf and Tauber ("Silicon Processing for the VLSI Era, Volume 1 – Process Technology," p.527-531).

25. In reference to claim 11, Hayashi does not disclose the use of TMAH as the developer. However the use of TMAH as a developer is well known in the art. Wolf and Tauber ("Silicon Processing for the VLSI Era, Volume 1 – Process Technology," p.527-531, hereinafter referred to as the "Wolf 1" reference) discloses that using TMAH as the developer has the benefits of sufficient sensitivity with high contrast and minimum erosion (p.530). Wolf 1 further discloses that these are desirable properties for a

developer (p.527-528). In view of Wolf 1, it would therefore be obvious to use TMAH as the developer in the device of Hayashi.

26. With regard to claim 12, the photoresist layer and the exposed region of the photosensitive layer are removed at the same time (column 11, lines 12-14).

27. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (USPN 5,717,251) in view of Wolf ("Silicon Processing for the VLSI Era, Volume 2 – Process Integration," p.273-275).

28. In reference to claim 15, Hayashi does not disclose the use of a passivation layer made of a stacked CVD oxide layer and a stacked CVD nitride layer. However the use of such a composite passivation layer is well known in the art. Wolf ("Silicon Processing for the VLSI Era, Volume 2 – Process Integration," p.273-276, hereinafter referred to as the "Wolf 2" reference) discloses that a passivation layer made of a stacked CVD oxide layer and a stacked CVD nitride layer (p.275) has the benefits of protecting against mechanical stress, handling, humidity, and mobile ions. Wolf 2 further discloses that these are desirable properties for a passivation layer (p.276). In view of Wolf 2, it would therefore be obvious to use a passivation layer made of a stacked CVD oxide layer and a stacked CVD nitride layer in the device of Hayashi.

29. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi et al. (USPN 5,717,251).

30. With regard to claim 22, Hayashi teaches all of the claimed invention except for the exact thickness of the photoresist layer. Although the Hayashi device does not teach the exact thickness as that claimed by Applicant:

> Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).
>
> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

Therefore claim 22 is not patentably distinguishable over the Hayashi reference.

Allowable Subject Matter

31. Claims 8 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

32. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a semiconductor device ands its fabrication process which forms a passivation layer over a circuit element but exposes it such that a photosensitive layer and a photoresist layer are formed above the exposed circuit element such that during the photoresist exposure and removal steps the photoresist prevents the photosensitive layer from being exposed but the photoresist itself is fully removed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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